REMARKS

Claims 1-20 were pending when last examined. Claims 21-31 have been withdrawn. With this Response, Applicant amends claim 1. All pending claims are shown in the detailed listing above.

Claim Rejections – 35 USC § 102

Claims 1-12 and 14-20 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Kledzik (US 5,266,912). Applicant respectfully traverses.

Claim 1 as amended recites *inter alia*, "a first ground plane coupled to the first IC chip" and "a second ground plane coupled to the second IC chip; wherein the first ground plane is physically separated and electrically isolated from the second ground plane." Such limitations are not disclosed or taught in Kledzik.

The Examiner states: "Kledzik teaches in col. 5/lls. 56-60, '*In some cases, additional layers of circuit traces 31, 32, and 33 may be incorporated into or below the substrate 17, in the configuration of a multilevel printed circuit board. In many cases, one layer, such as layer 33, is configured as a ground plane. In this manner, the module 11 can be constructed with a controlled electrical impedance, as determined by various factors*'. In this case, any layer connected to the layer 33 in the same substrate or in other substrate is recognized as ground plane because is connected to the ground." Office Action, pp. 5-6.

Although the Applicant does not necessarily agree with this statement by the Examiner, even if such statement is accepted to be true, then Kledzik most certainly does not disclose or teach a first ground plane which is physically separated and electrically isolated from a second ground plane. Indeed, Kledzik is teaching exactly the opposite--i.e., a single ground plane that is formed by all of the layers which are electrically connected to the ground layer 33. As such, the limitations of "a first ground plane coupled to the first IC chip" and "a second ground plane coupled to the second IC chip; wherein the first ground plane is physically separated and electrically isolated from the second ground plane" as

recited in Applicant's claim 1 is not disclosed or taught by Kledzik. Thus, Kledzik does not anticipate claim 1.

For at least the reasons discussed above, Applicant respectfully requests that the rejection of claim 1 under 35 U.S.C. § 102(b) be withdrawn and this claim be allowed. Furthermore, because claims 2-12 and 14-20 depend from claim 1 and include further limitations, the Applicant respectfully requests that the rejection of these dependent claims under 35 U.S.C. § 102(b) also be withdrawn and that claims 2-12 and 14-20 be allowed.

Claim Rejections – 35 USC § 103

Claim 13 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kledzik in view of excerpts from Wolf, *Silicon Processing For the VLSI Era*, Vol. 1, 2d ed. (2000). Applicant respectfully traverses.

Claim 13 depends from claim 1, which include limitations not disclosed in Kledzik, as discussed above. Nor are such limitations disclosed or taught in Wolf, taken alone or in combination with Kledzik. Accordingly, claim 13 is not rendered obvious by the cited art.

For at least the reasons discussed above, Applicant respectfully requests that the rejection of claim 13 under 35 U.S.C. § 103(a) be withdrawn and this claim be allowed.

CONCLUSION

Applicant respectfully requests that the pending claims be allowed and the case passed to issue. Should the Examiner wish to discuss the Application, it is requested that the Examiner contact the undersigned at (415) 772-7428.

Certificate of Mailing

I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

9/27/07 Richard A. Pask

Date Signature

Respectfully submitted,

By: _____

Philip W. Woo
Attorney of Record
Reg. No.: 39,880
PWW/rp

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SIDLEY AUSTIN LLP
555 California Street, Suite 2000
San Francisco, CA 94104-1715